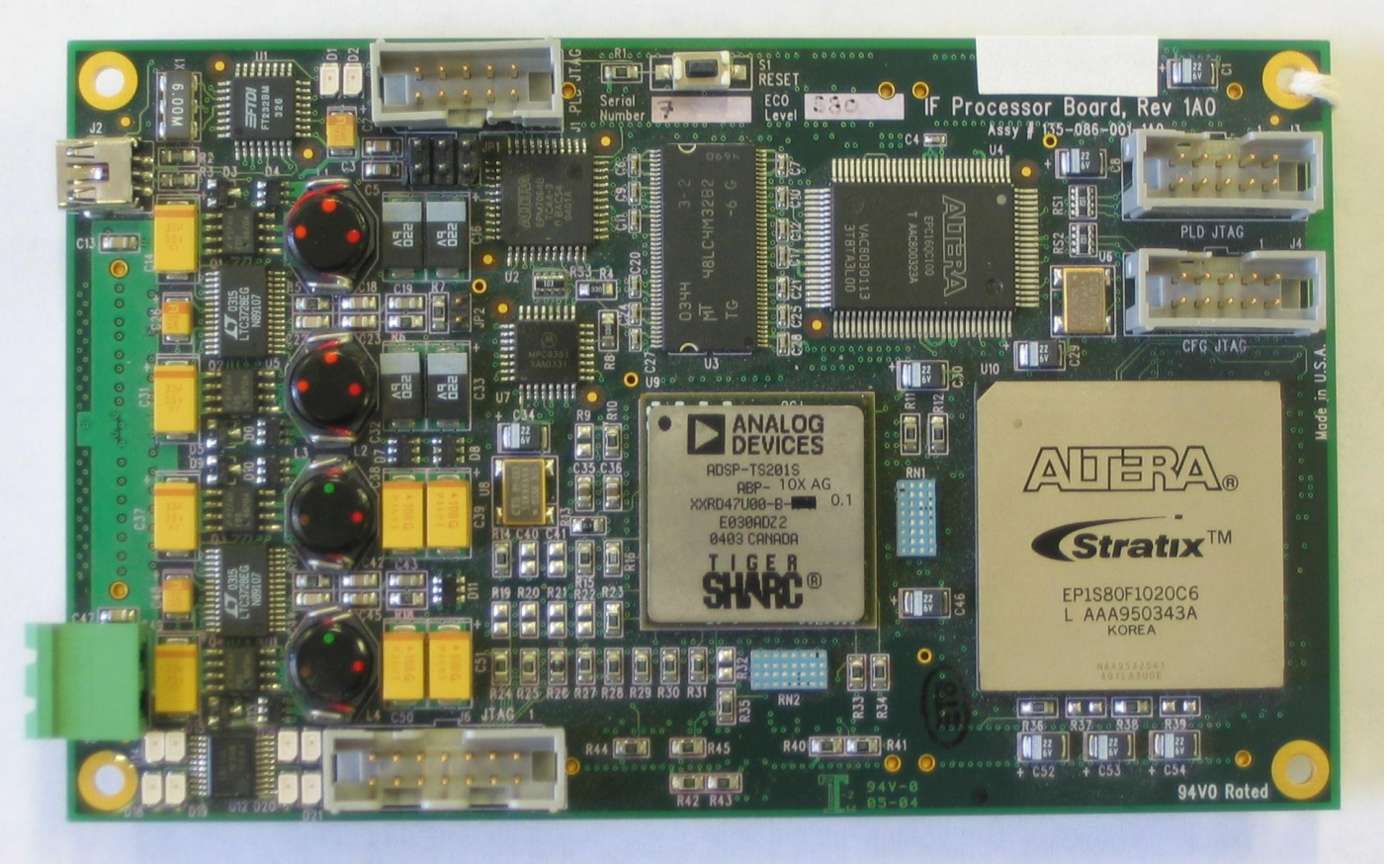

RF Power Amplifier Predistortion Engine

Background

A client was developing a unique RF Power Amplifier that monitored its own output and fed back information to predistort the transmitted signal so as to reduce the overall system distortion. The system incorporated a proprietary Programmable Logic Device (PLD) computational engine that modeled the output amplifier's transfer characteristics and calculated a real-time pre-distorted signal to cancel out the distortion introduced by the power amplifier. The client's computational engine required tens of billions of operations per second to accurately model the amplifier characteristics. A high speed floating point DSP calculated, managed and logged the data required to update the processing engine coefficients thousands of times a second. The client hired Bolton Engineering to construct the hardware on which their algorithms would run.

System Overview

The full RF Power Amplifier Predistortion Engine incorporated two DSP boards, a baseband RF board, and the RF Amplifier subsystem. Bolton Engineering designed the DSP boards, plus the baseband board, and the client designed the RF Amplifier subsystem

The DSP board incorporated 32Megabytes of SDRAM, an Analog Devices TigerSHARC processor capable of performing 4.8 billion Multiply-Accumulate (MAC) cycles per second, 16Megabytes of Flash memory, a USB port to a host computer, a variety of system I/O interfaces, a clock distribution chip, and four sequenced power supplies plus sequencing logic.

The Bolton-designed Baseboard RF board (not shown) incorporated a 105MHz 14-bit A/D and a 500MHz interpolating 16-bit D/A, a low-jitter clock distribution system, several high-resolution RTD temperature sensor interfaces, a system monitor A/D, several D/A ports, and various other system interfaces. The TigerSHARC processors communicated to each other and to the PLDs via their high-speed LVDS (Low Voltage Differential Signaling) Link Ports.

Project Scope

Bolton Engineering wrote the specification, designed the schematics, designed the 10-layer DSP System circuit board, designed the 6-layer RF Baseband circuit board, designed and debugged major sections of the PLD, implemented the PLD-based Link Port interfaces, rewrote defective PLD Link port code, wrote diagnostic and driver software in 'C', debugged the system, and delivered ten working prototypes. The client developed and maintained the PLD code for their proprietary predistortion computation engine.

2 Connector Rd, Andover MA 01810, tel: (978) 474-0600